

[Apr-24]

GITAM (Deemed to be University)
[CSEN2011]
GST/GSS/GSB/GSHS Degree Examination

IV Semester

COMPUTER ORGANIZATION AND ARCHITECTURE
(Effective from the admitted batch 2021-22)

Time: 2 Hours

Max. Marks: 30

Instructions: All parts of the unit must be answered in one place only.

Section-A

1. **Answer all questions:** (5×1=5)

- a) Discuss on i) Micro Operation ii) Register transfer language
- b) What does this mean: $T0: R4 <- R0$?
- c) Evaluate $X = (A + B) * (C + D)$ in Three Address Instruction Format.
- d) Classify the Printable characteristics of ASCII.
- e) Demonstrate the Memory Hierarchy.

Section-B

Answer the following: (5×5=25)

UNIT-I

2. An 8-bit register contains the binary value 11100101. Evaluate the register value after an arithmetic shift right , arithmetic shift left logical shift right , logical shift left.

OR

3. Demonstrate and Explain 4-bit Adder-Subtractor circuit with function table.

UNIT-II

4. Perform the following logical applications, when register A contains 1011 and register B is a logic operand 1010

- i) selective -set
- ii) selective- clear
- iii) selective – complement
- iv) clear

OR

5. Explain about Memory Reference instructions.

UNIT-III

6. An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is: i) Immediate ii) Direct iii) Register indirect iv) Relative v) Index with R1 as the index register.

OR

7. Discuss Data Manipulation instructions with examples.

UNIT-IV

8. What is the use of Asynchronous data transfer(ADT)? Explain various data transfer approaches of ADT, With suitable diagram.

OR

9. What is DMA and explain its procedure?

UNIT-V

10. Draw the memory connections to the CPU512 bytes of RAM and 512 bytes of ROM. (Available chips are 512 X 8 ROM and 128 x8 RAM).

OR

11. Discuss various mapping procedures of cache memory with suitable figures.

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