[Apr-24]

GITAM (Deemed to be University)
[CSEN2011]
GST/GSS/GSB/GSHS. Degree Examination

IV Semester

COMPUTER ORGANIZATION AND ARCHITECTURE

(Effective from the admitted batch 2021–22)

Time: 2 Hours **Max.Marks: 30**

Instructions: All parts of the unit must be answered in one place only.

Section-A

1. Answer all Questions: **(5×1=5)**

a) The Processor contains several special purpose registers. One such register is Program Counter (PC). What is the function of PC and what is the initial value stored in PC just before the start of the Program execution?

b) Discriminate the memory reference instructions from the register reference instructions.

c) Compare the performance of pipelined processor with non-pipelined processor using suitable equation.

d) List the three possible modes of data transfer to and from the peripheral.

e) Distinguish between RAM and ROM.

Section-B

Answer the following: **(5×5=25)**

UNIT-I

2. Register R1 contains 1111 0101 and R2 contains 0100 0010. The following operations are performed R1← ashr R1; R2 ←ashr R2. Write the content of R1 and R2 after the shift operation. Also, write the decimal equivalent of the registers before and after the shift operations.

OR

3. Demonstrate the role of Multiplexer in establishing common Bus system for connecting four registers.

UNIT-II

4. Write the micro-instruction format and the symbolic Micro-program for the Fetch routine.

OR

5. Explain about Interrupt cycle and draw complete flowchart for instruction cycle which includes interrupt cycle also.

UNIT-III

6. Assume that a processor has four stage pipeline for the execution of instructions. Each stage has delay of 100 ns. Calculate the execution time of 1000 instructions executed using a (i) Processor that employed Pipeline for the instruction execution (ii) Processor without Pipeline (iii) Speed Up achieved using pipeline.

OR

7. Write Assembly level code to evaluate X=(A*B)-(C+D) expression considering one address instructions and zero address instructions.

UNIT-IV

8. Explain the three possible errors that may occur during data transmission.

OR

9. What is DMA and explain the two modes of DMA operation.

UNIT-V

10. With neat diagram explain Organization and working of Content Addressable Memory(CAM).

OR

11. Distinguish the Write-through from Write-back policy used while updating the cache.